Module 1
Introduction and Overview of Computer Architecture
Part B

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Topics Covered (Module 1 Part B)

- Overview of IAS computer function
- Von Neumann Machine
- Harvard Architecture
- CISC & RISC Architectures

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Important facts about IAS computer

- The memory contains words that basically represents data or instruction.
- The basic data is a binary number in IAS computer.
- IAS instructions are 20 bits long.
- Instruction in IAS consists of two parts - 1) operation code or op-code which is of 8-bit. 2) address of 12-bit
- IAS instruction allow only one memory address.
- The IAS computer has CPU.
- CPU consists of program control unit and data processing unit. It also contains control unit along with various set of high speed registers. These registers are meant for temporary storage of instructions and data.
- The main memory is used for storing programs and data.

Stored Program Concept

•Stored program concept is introduced by John von Neumann in 1940s.

•The idea of a stored program is to store the instructions and data electronically as binary numbers in a storage space associated with a computer.

•The storage space is called as memory.

•Any data such as input or instruction is stored as a binary number in the memory.

There is a Need for Stored Program & Processing Machine

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How to implement the Stored-Program Concept in reality?

SOLUTION:

- Von Neumann Architecture
- Harvard architecture

Organization of Von Neumann machine

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Von Neumann machine

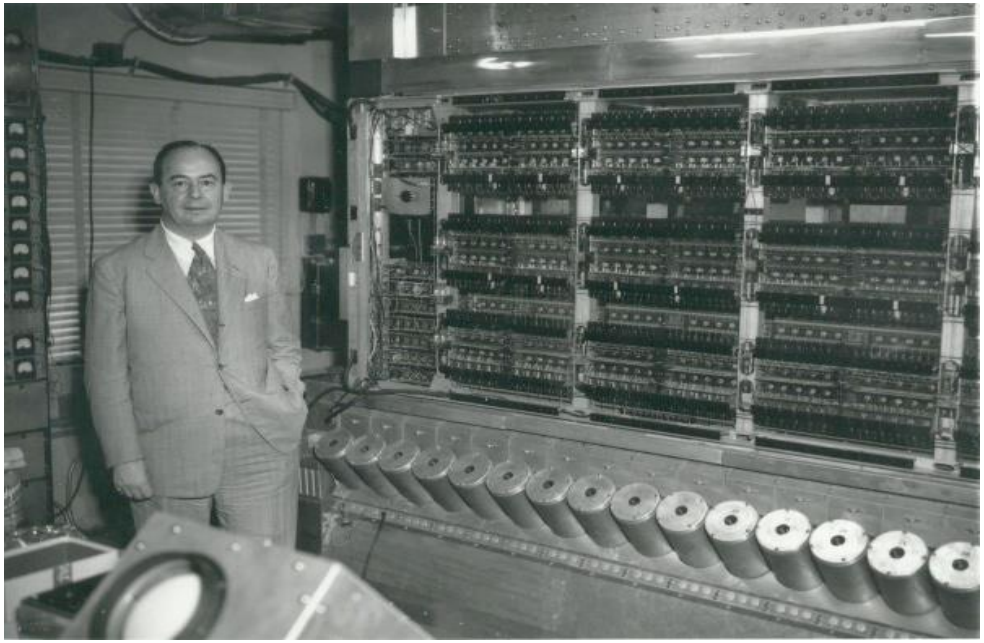
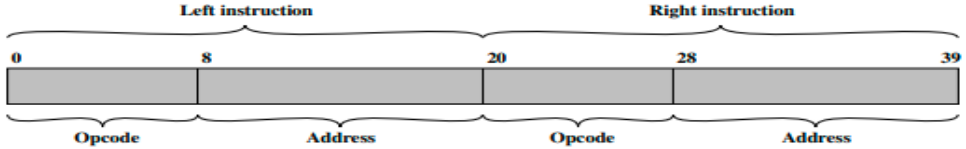


Image courtesy: www.medium.com

- Developed by John Von Neumann in 1940 in Princeton University, in Institute of Advanced Sciences (IAS)

Von Neumann architecture

- Von Neumann architecture has common memory space to store both program and data memory- uses Stored Program concept
- Fetches instructions and data from one memory
- Limits operating bandwidth
- One piece of data or one instruction at a time



(b) Instruction word

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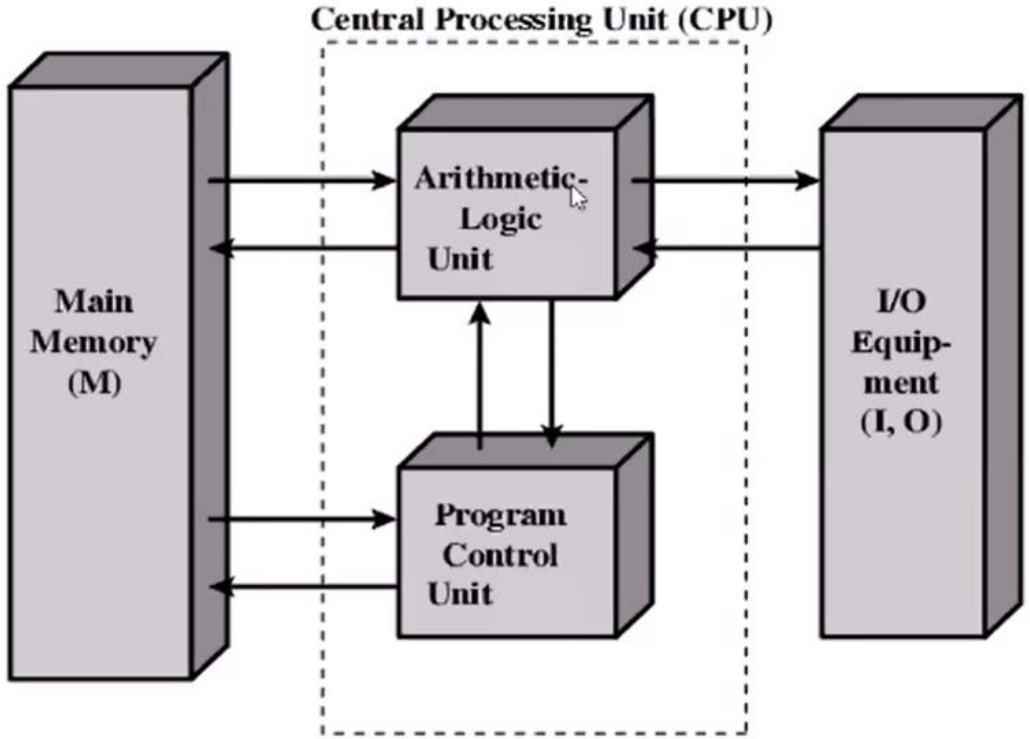
Structure of Von Neumann Machine

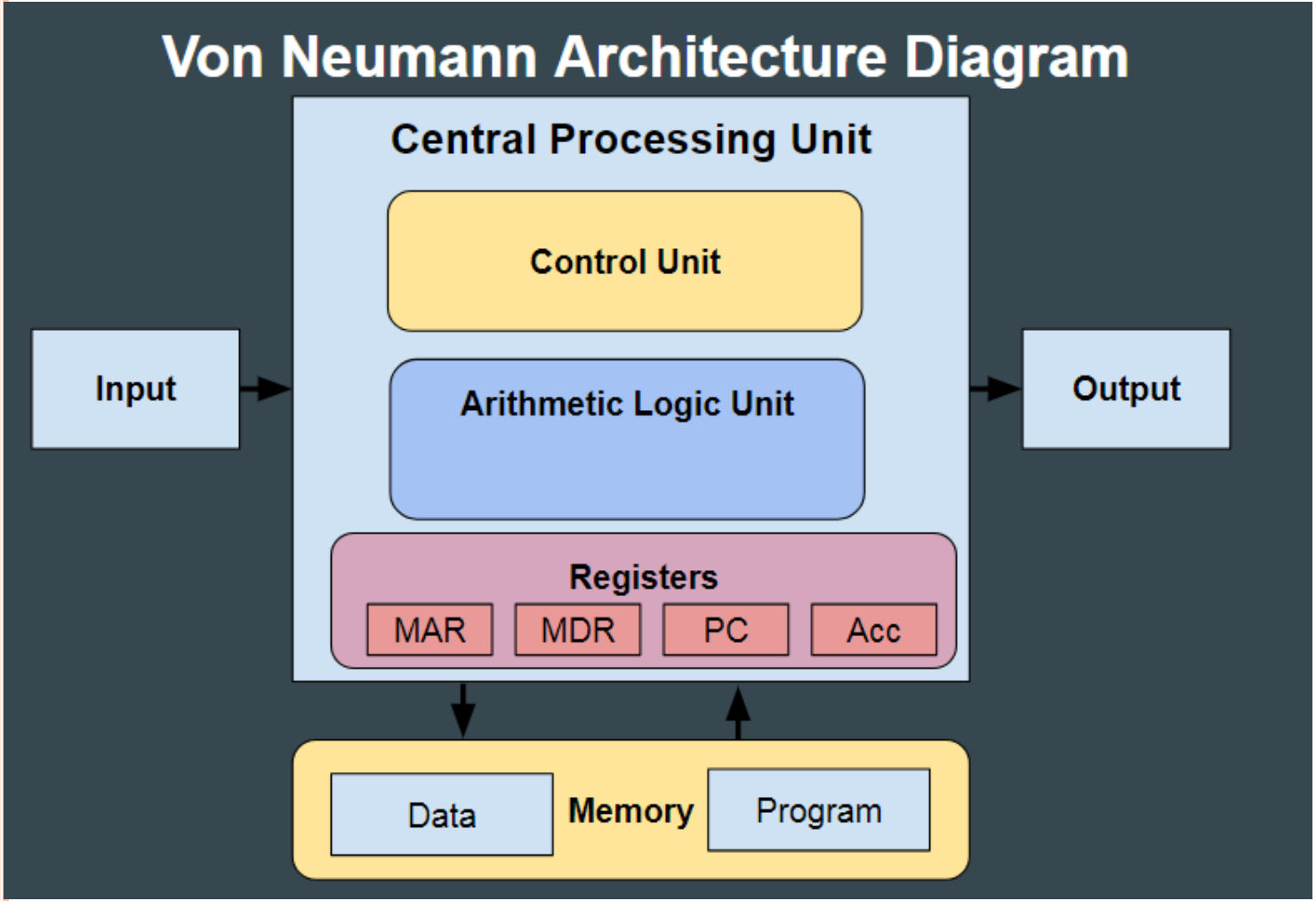


TYPES OF INSTRUCTIONS

- **Data Transfer Instructions** – transfers data from a source to a destination. The source and destination can be memory locations or registers that are associated with CPU.

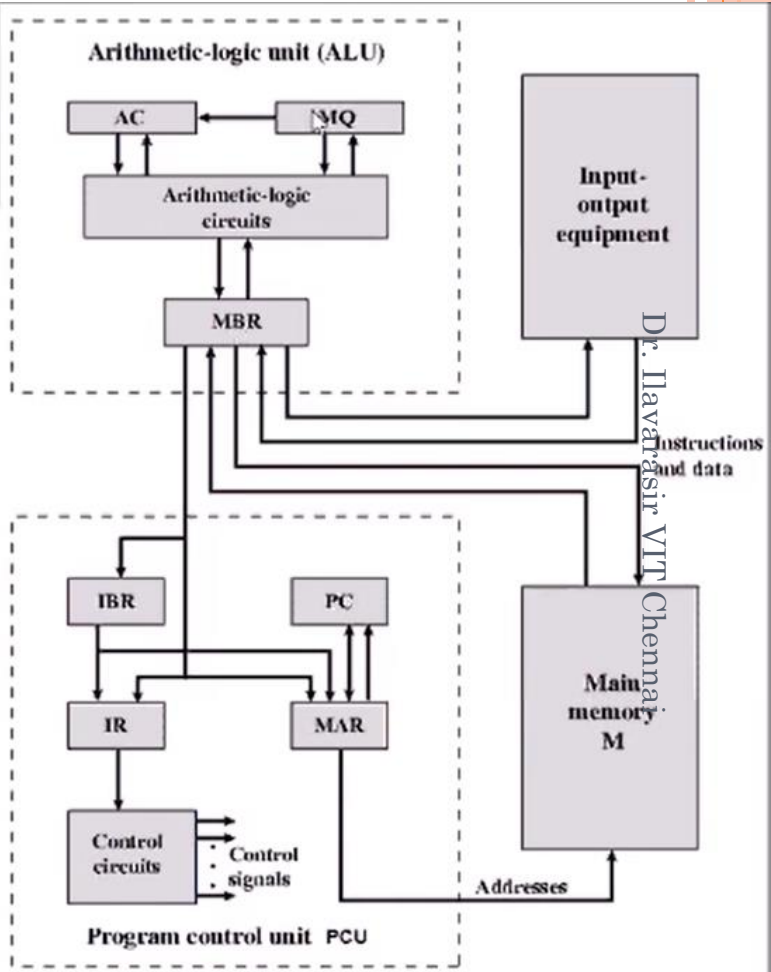
- **Arithmetic Instructions**–performs arithmetic operations such as addition, subtraction, multiplication, division etc. It is performed by ALU.
- **Logical Instructions-** Performs logical operations

- **Control transfer instructions** – The flow of sequential execution can be changed with a branch instruction, it can be made according to any condition.


Von Neumann Architecture Diagram
Central Processing Unit
Control Unit
Arithmetic Logic Unit
Registers
MAR
MDR
PC
Acc
Input
Output
Data
Memory
Program

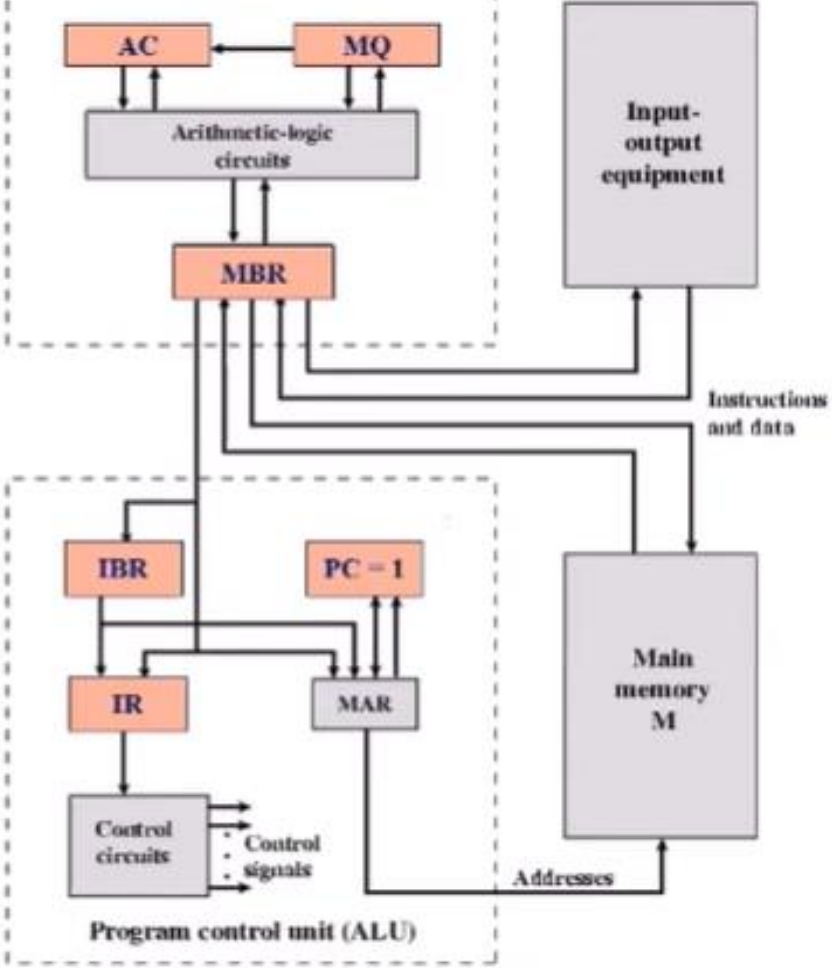
Von Neumann Machine

- **MBR: Memory Buffer Register**
  - contains the word to be stored in memory or just received from memory.
- **MAR: Memory Address Register**
  - specifies the address in memory of the word to be stored or retrieved.
- **IR: Instruction Register** - contains the 8-bit opcode currently being executed.
- **IBR: Instruction Buffer Register**
  - temporary store for RHS instruction from word in memory.
- **PC: Program Counter** - address of next instruction-pair to fetch from memory.
- **AC: Accumulator & MQ: Multiplier quotient** - holds operands and results of ALU ops.



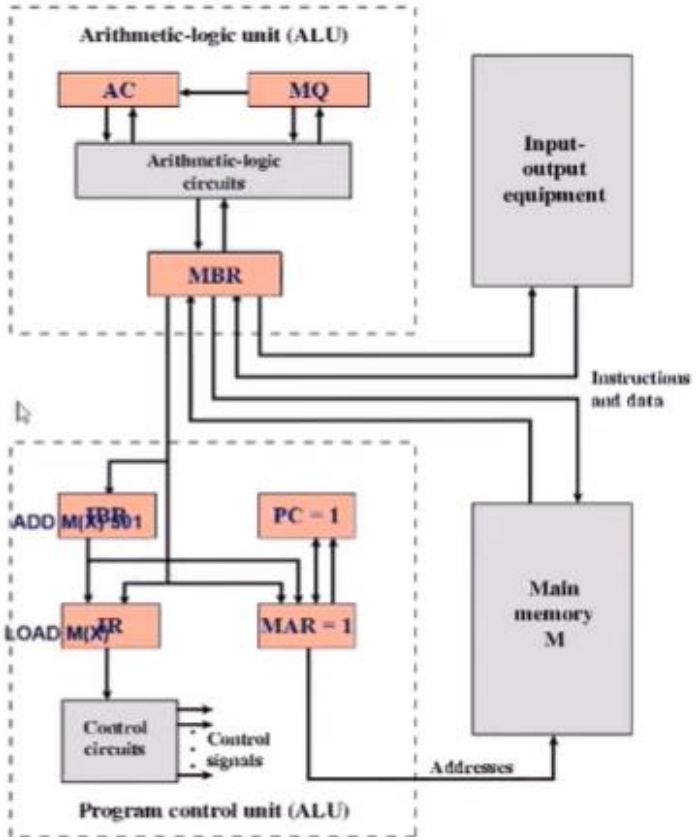
MEMORY
1. LOAD M(X) 500, ADD M(X) 501
2. STOR M(X) 500, (Other Ins)
.....
500. 3
501. 4

PC	1
MAR	
MBR	
IR	
IBR	
AC	



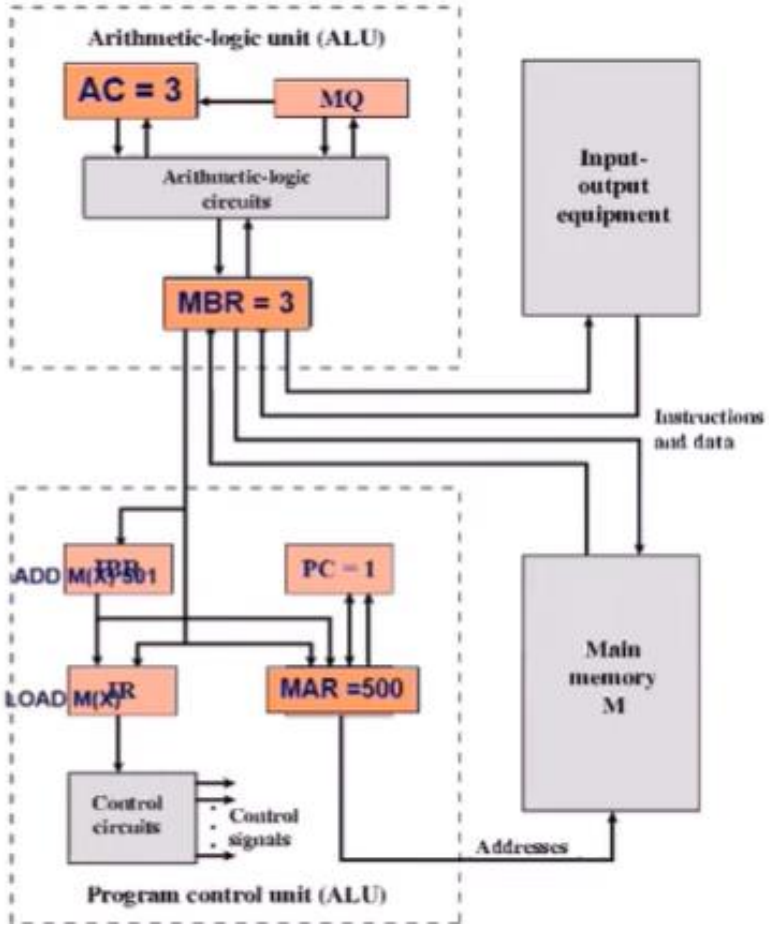
MEMORY
1. LOAD M(X) 500, ADD M(X) 501
2. STOR M(X) 500, (Other Ins)
.....
500. 3
501. 4

PC	1
MAR	1
MBR	LOAD M(X) 500, ADD M(X) 501
IR	LOAD M(X)
IBR	ADD M(X) 501
AC	



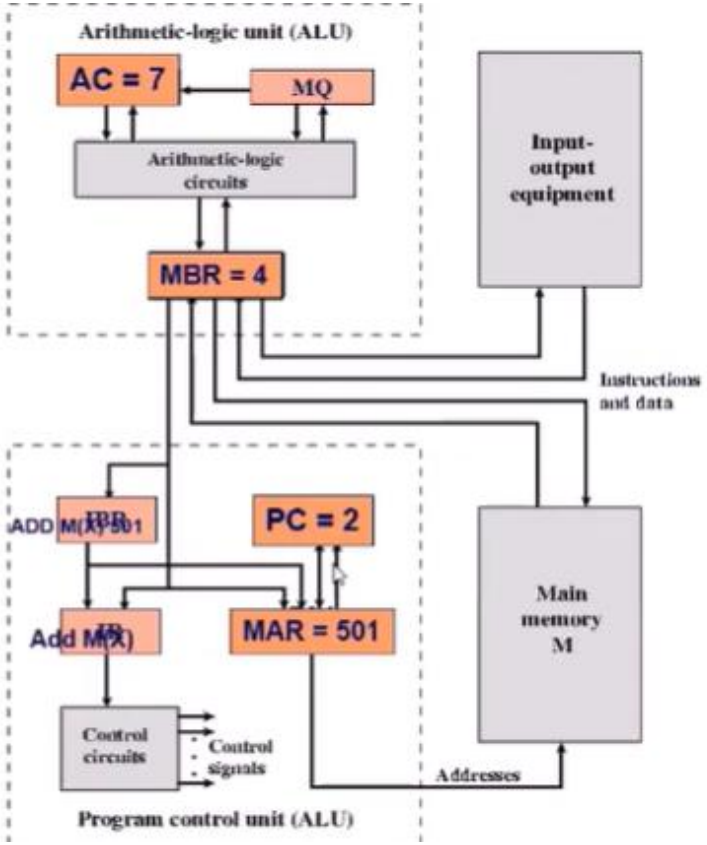
MEMORY
1. LOAD M(X) 500, ADD M(X) 501
2. STOR M(X) 500, (Other Ins)
.....
500. 3
501. 4

PC	1
MAR	500
MBR	3
IR	LOAD M(X)
IBR	ADD M(X) 501
AC	3



MEMORY
1. LOAD M(X) 500, ADD M(X) 501
2. STOR M(X) 500, (Other Ins)
.....
500. 3
501. 4

PC	2
MAR	501
MBR	4
IR	ADD M(X)
IBR	ADD M(X) 501
AC	7



MEMORY
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PC	2
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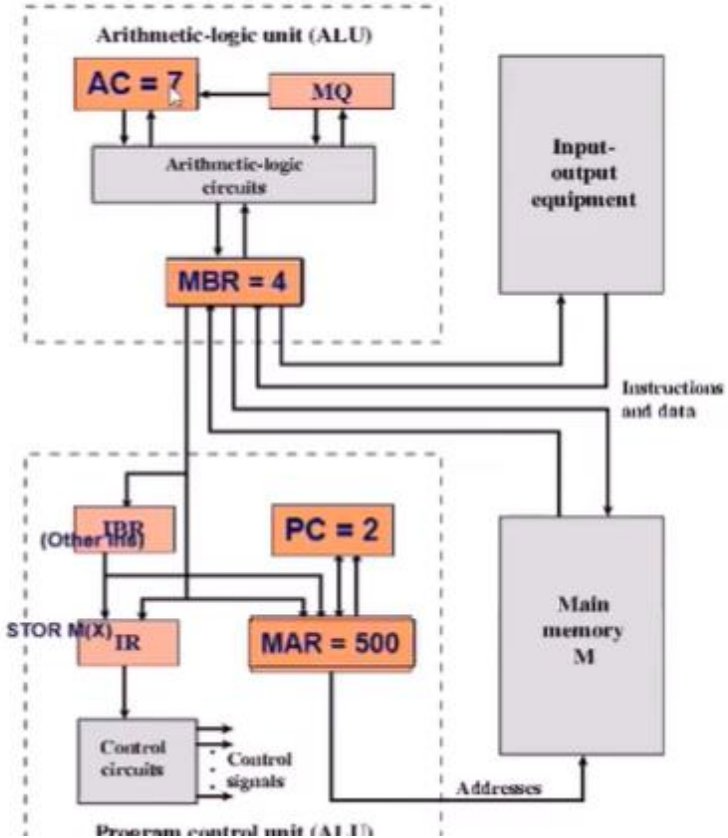
AC	7



MEMORY
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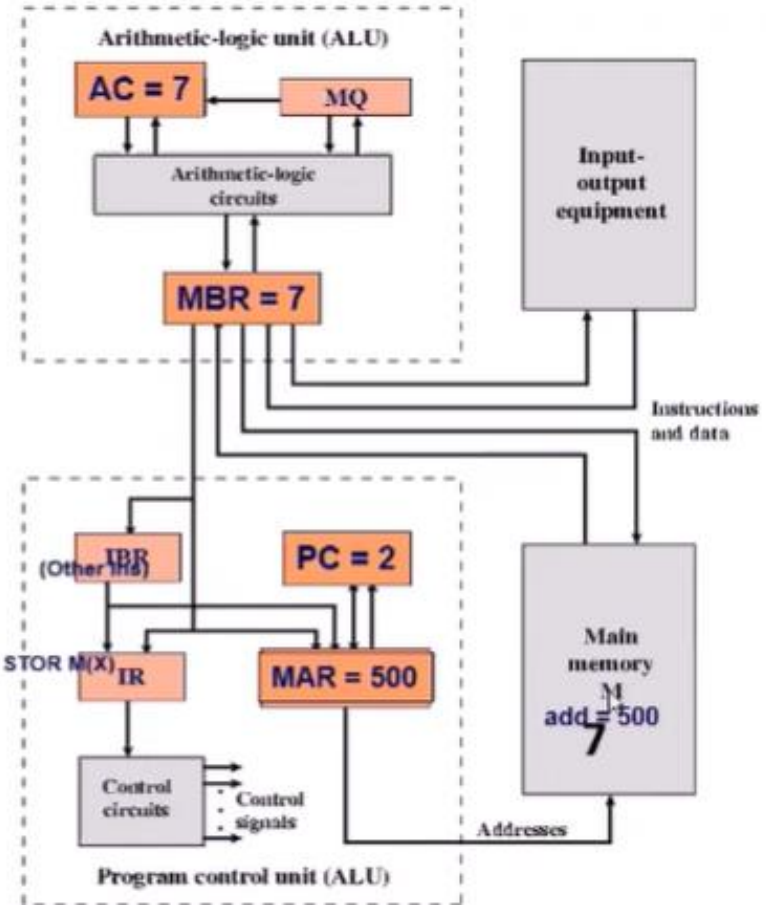

Register Transfer Operations

1. LOAD M(X) 500, ADD M(X) 501 (PC = 1)

- MAR ← PC
- MBR ← M[MAR]
- IBR ← MBR[20:39]
- IR ← MBR[0:7]
- MAR ← MBR[8:19]
- MBR ← M[MAR]
- AC ← MBR
- IR ← IBR[0:7]
- MAR ← IBR[8:19]
- PC ← PC + 1
- MBR ← M[MAR]
- AC ← AC + MBR

2. STOR M(X) 500, (Other Ins)

- MAR ← PC
- MBR ← M[MAR]
- IBR ← MBR[20:39]
- IR ← MBR[0:7]
- MAR ← MBR[8:19]
- MBR ← AC
- M[MAR] ← MBR

Harvard Architecture

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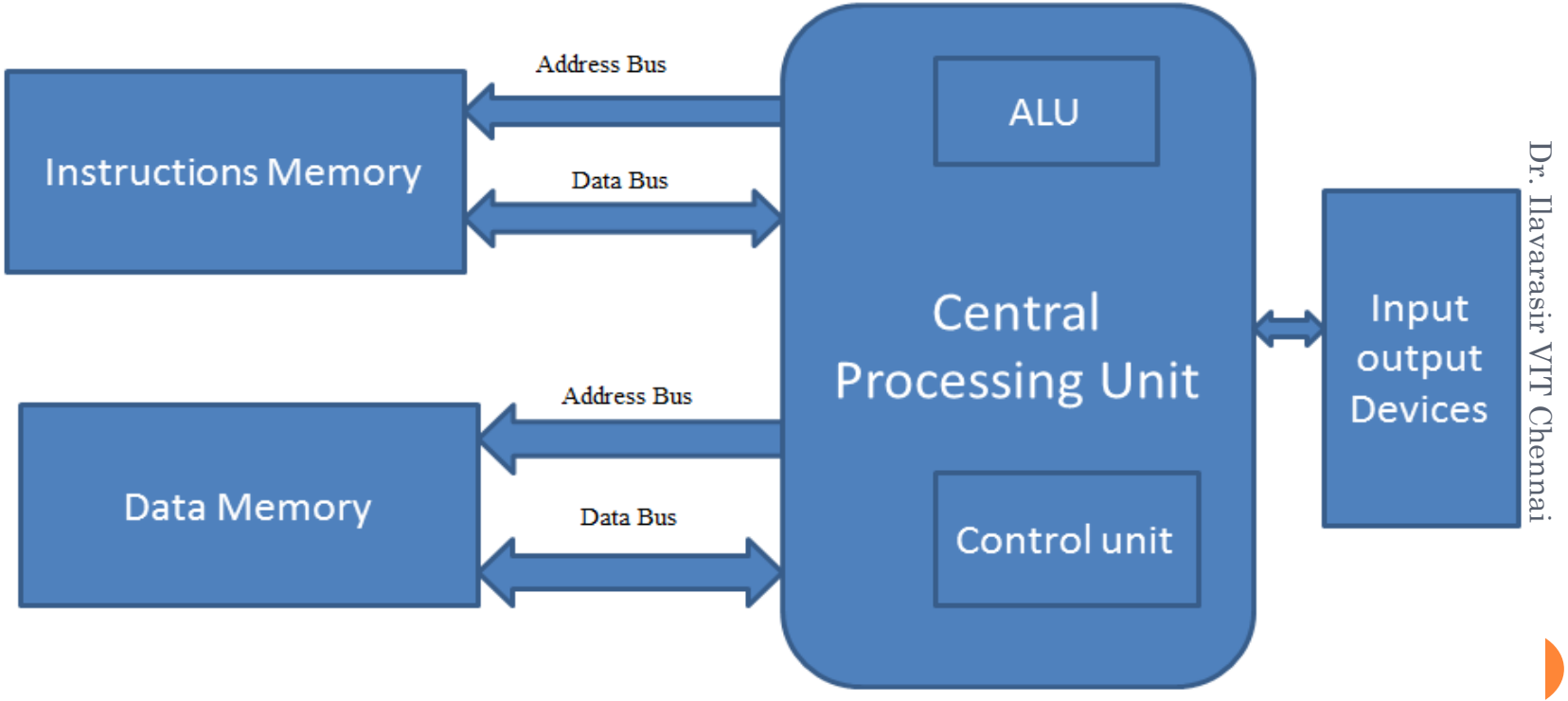
Harvard Architecture

- Principles
  - In Harvard architecture concept, Memory for data was separated from the memory for instruction.
  - This concept is known as the Parallel access of data and instructions are possible Modern processors uses Harvard architecture

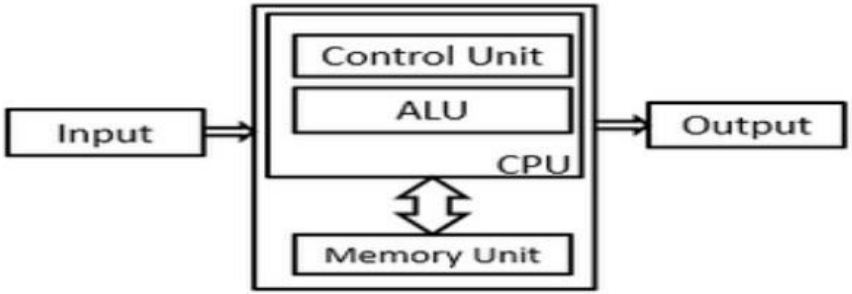
Harvard Architecture



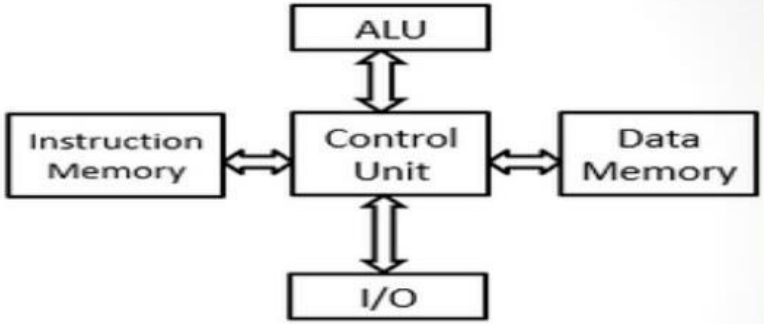
Features of Harvard Architecture

- Separate data path and instruction path is available.
- Fetching of data and instructions can be done simultaneously
- Different sized cells can be allowed in both the memories.
- Both memories can use different cell sizes making effective use of resources.
- Greater memory bandwidth that is more predictable (separate memory for instructions and data)
- There is less chance of corruption since data and instructions are transferred via different buses

Von Neumann vs. Harvard architectures



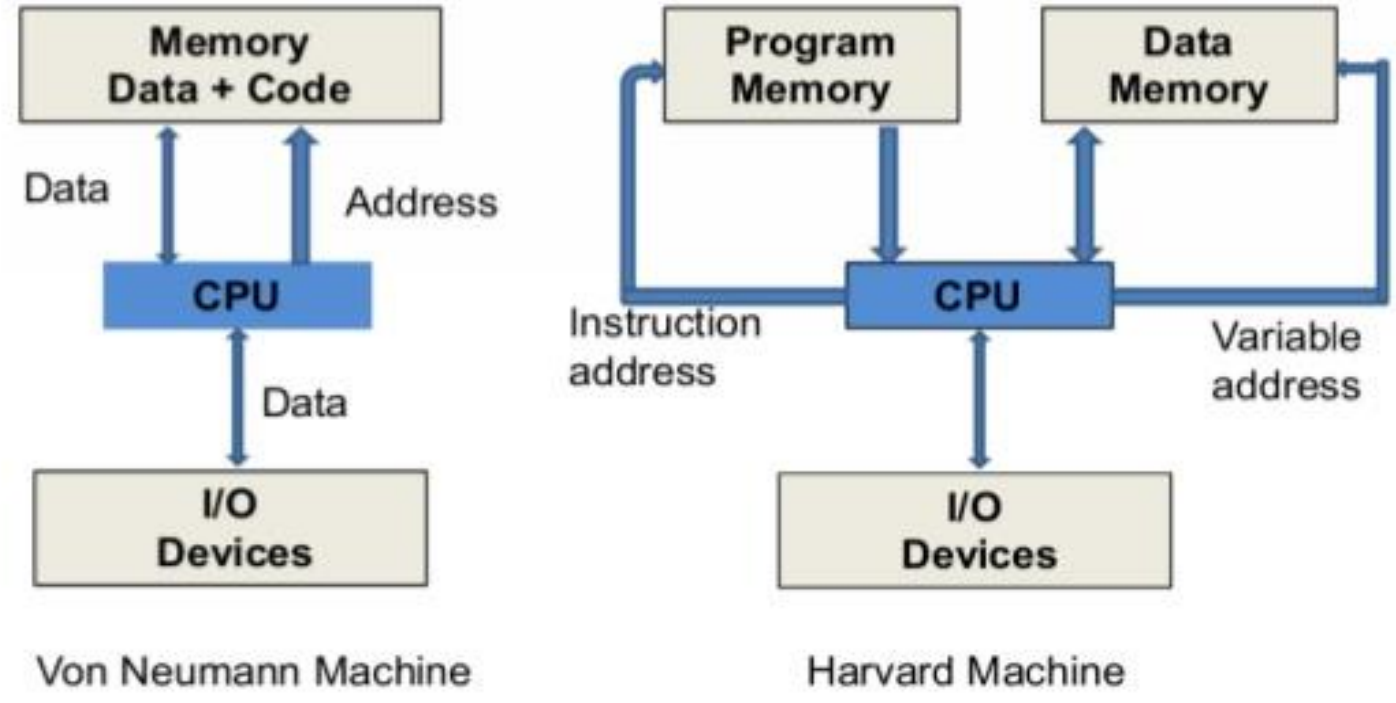
Von Neumann Model



Harvard Model

Von Neumann and Harvard Architecture

Von Neumann vs. Harvard Architecture



Von Neumann Machine

Harvard Machine

Comparison of von Neumann and Harvard Architecture

Von Neumann Architecture	Harvard Architecture
It is a conceptual design based on stored program architecture	It is a modern computer architecture
Memory is common for both instruction and data	Separate memory is there for instruction and data
Common bus between memory and CPU for both instruction and data	Separate buses for instruction memory and data memory
Two clock cycles required for the processor to execute an instruction	Only one clock cycle is enough for the processor to execute an instruction
Data transfer and instruction fetches cannot be done simultaneously	Data transfer and instruction fetches can be done simultaneously
Control unit design is simple	Control unit for two buses is more complicated which increses the development cost

RISC and CISC Architectures

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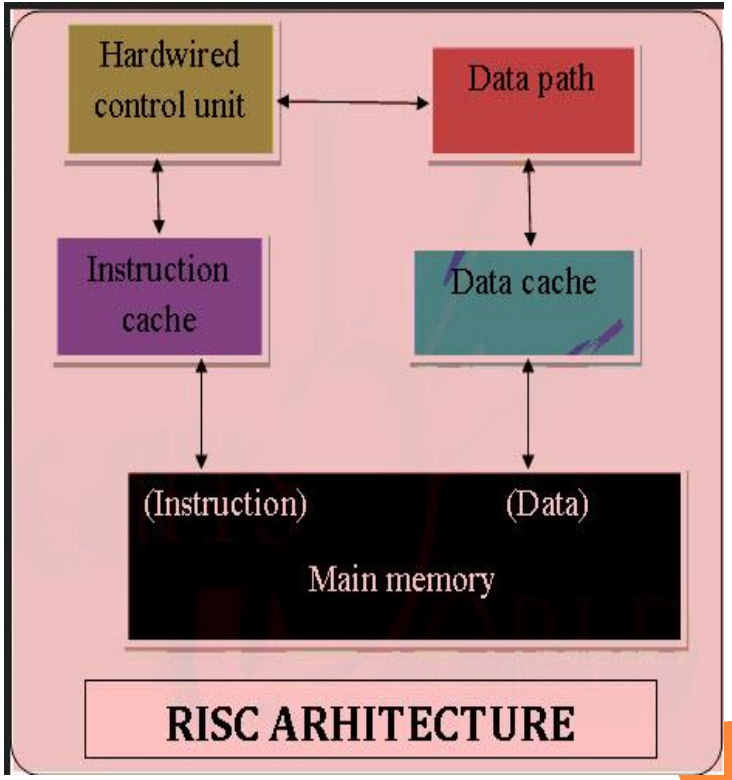
RISC (Reduced Instruction Set Computer)

- To execute each instruction, if there is separate electronic circuitry in the control unit, which produces all the necessary signals, this approach of the design of the control section of the processor is called RISC design. It is also called hard-wired approach.
- Examples of RISC processors: IBM RS6000, MC88100; DEC's Alpha 21064, 21164 and 21264 processors
- It is a highly customized set of instructions used in portable devices due to system reliability such as Apple iPod, mobiles/smartphones, Nintendo DS

RISC Features

- RISC processors use a small and limited number of instructions
- RISC machines mostly uses hardwired control unit.
- RISC processors consume less power and are having high performance.
- Each instruction is very simple and consistent. RISC processors uses simple addressing modes.

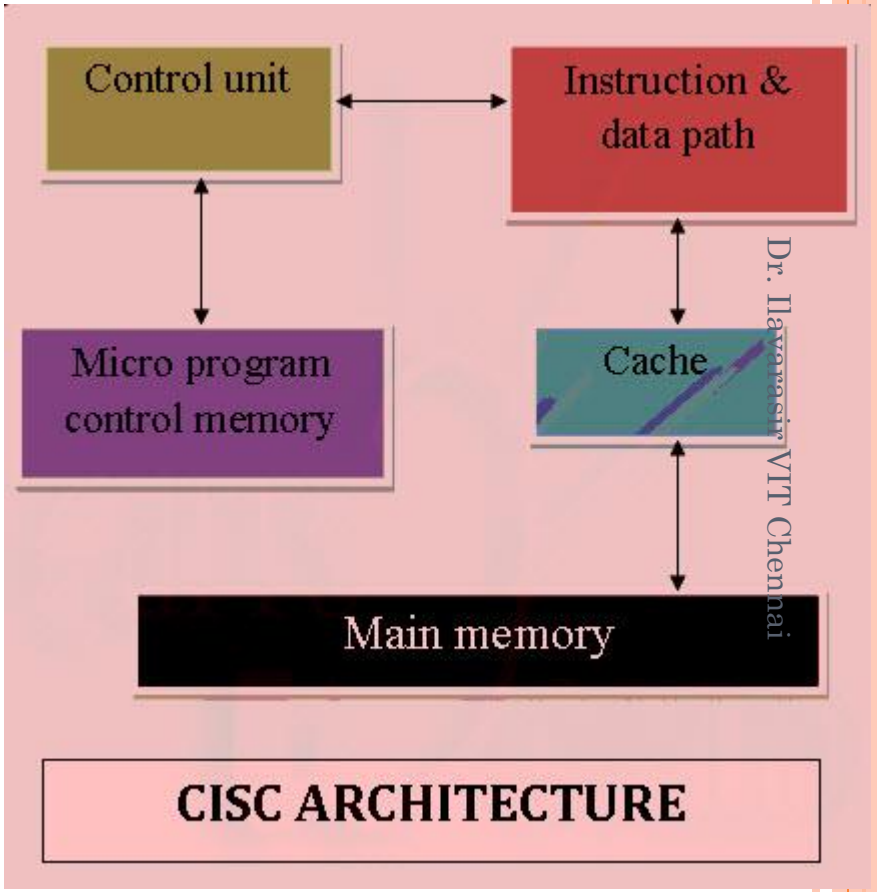


CISC (Complex Instruction Set Computer)

- If the control unit contains a number of microelectronic circuitry to generate a set of control signals and each micro-circuitry is activated by a microcode, this design approach is called CISC design.
- Examples of CISC processors are: Intel 386, 486, Pentium, Pentium Pro, Pentium II, Pentium III ; Motorola's 68000, 68020, 68040, etc.
- It has a large collection of complex instructions that range from simple to very complex and specialized in the assembly language level, which takes a long time to execute the instructions.

CISC Feature

- CISC chips have a large amount of different and complex instructions. Code size is compact.
- CISC machines generally make use of complex addressing modes.
- Different machine programs can be executed on CISC machine.
- CISC machines uses micro-program control unit.
- CISC processors are having limited number of registers.



RISC vs. CISC

CISC	RISC
Emphasis on hardware	Emphasis on software
Multiple instruction sizes and formats	Instructions of same set with few formats
Less registers	Uses more registers
More addressing modes	Fewer addressing modes
Extensive use of microprogramming	Complexity in compiler
Instructions take a varying amount of cycle time	Instructions take one cycle time
Pipelining is difficult	Pipelining is easy

THANK YOU

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